

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE PATENT APPLICATION

In re Application of:

Pendharker et al.

Atty. Docket: TI-33654

Serial No.:

10/678,028

Art Unit: TBD

Filed:

09/29/2003

Examiner: TBD

For:

A LOW NOISE VERTICAL VARIABLE GATE CONTROL VOLTAGE JFET DEVICE IN A BICMOS PROCESS AND

METHODS TO BUILD THIS DEVICE

Commissioner for Patents

Alexandria, VA 22313-1450

P. O. Box 1450

CERTIFICATE OF MAILING OR TRANSMISSION

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INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO-1449. Copies of the noted documents are enclosed. Please charge any necessary fees to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. Charge any additional fee required or credit any overpayment to the same.

Respectfully submitted

Attorney for Applicant(s

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					APPLICANT Pendharkar et al.					
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U.S. PATENT DOCUMENTS *EXAMINER DOCUMENT										
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)										
Pending U.S. Application No. 10/623,230 (TI-35213), Howard et al. "Double Diffused Vertical JFET"										
Pending U.S. Application No. 10/614,840 (TI-35193), Howard et al. "Implant-Controlled-Channel Vertical JFET"										
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EXAMINER DATE CONSIDERED										
*EXAMINER: Initial	if reference co	onsidered, whether or not citation	is in conformance	with MPEP 609;	Draw line thro	ugh citation if not in	n conform	ance and no	t considered. Include copy	